

IN THE CLAIMS:

1. (Currently Amended) A method of forming semiconductor devices having field isolation layers in trenches, comprising:
 - providing a semiconductor substrate that includes a cell region and a high voltage region;
 - forming a pilot trench at a location in the high voltage region;
 - concurrently forming an upper trench, a bottom trench in the high voltage region, and a trench in the cell region, the upper trench substantially centered at the location of the pilot trench, the bottom trench having a top at substantially the same level as a bottom surface of the upper trench, and the upper trench having a wider width than that of the bottom trench;
 - and
 - forming a field isolation layer filling the bottom trench and the upper trench.
2. (Previously presented) The method as claimed in claim 1, wherein concurrently forming the upper trench and bottom trench comprises:
 - forming a trench mask layer on the semiconductor substrate having the pilot trench;
 - forming an opening exposing the pilot trench and a predetermined region of the semiconductor substrate at both sides of the pilot trench by patterning the trench mask layer;
 - and
 - forming the upper trench and the bottom trench by anisotropically etching the exposed bottom surface of the pilot trench and the semiconductor substrate,
wherein the upper trench has substantially the same width as the opening and the bottom trench has substantially the same width as the pilot trench.
3. (Previously presented) The method as claimed in claim 2, further comprising forming a channel stop impurity-doped region in the semiconductor substrate apart from the bottom surface of the pilot trench with a predetermined depth, wherein the bottom surface of the bottom trench is in contact with the channel stop impurity-doped region.
4. (Previously presented) The method as claimed in claim 3, wherein the pilot trench has substantially the same width as the channel stop impurity-doped region.

5. (Previously presented) The method as claimed in claim 4, wherein forming the pilot trench and the channel stop impurity-doped region comprises:

- forming a pilot trench mask layer on the semiconductor substrate;
- forming a pilot trench opening exposing a predetermined region of the semiconductor substrate by patterning the pilot trench mask;
- forming the pilot trench by selectively etching the exposed semiconductor substrate;
- forming a channel stop impurity-doped region in the semiconductor substrate apart from the bottom surface of the pilot trench with a predetermined depth by implanting impurity ions using the patterned pilot trench mask layer as a mask; and
- removing the patterned pilot trench mask layer.

6. (Previously presented) The method as claimed in claim 3, wherein the pilot trench has a wider width than the channel stop impurity-doped region.

7. (Currently Amended) The method as claimed in claim 6, wherein forming the channel stop impurity-doped region comprises:

- forming an ion-implantation mask layer on the semiconductor substrate having the pilot trench;
- forming an ion-implantation opening having a narrower width than that of the pilot trench and exposing a bottom predetermined region of the pilot trench by patterning the ion-implantation mask layer;
- forming a channel stop impurity-doped region in the semiconductor substrate apart from the bottom surface of the pilot trench by implanting impurity ions using the patterned ion-implantation mask as a mask; and
- removing the patterned ion-implantation mask.

8. (Previously presented) The method as claimed in claim 2, wherein forming the field isolation layer comprises:

- forming a field insulator filling the upper trench and the bottom trench on a surface of the semiconductor substrate;
- planarizing the field insulator until the patterned trench mask layer is exposed; and
- removing the exposed trench mask layer.

9. (Currently Amended) The method as claimed in claim 1, wherein concurrently forming the upper trench and the bottom trench comprises: forming the upper trench at a predetermined region of the semiconductor substrate; and concurrently forming the bottom trench by selectively etching a ~~bottom~~ predetermined bottom region of the pilot trench.

10. (Original) The method as claimed in claim 9, further comprising forming a channel stop impurity-doped region in the semiconductor substrate under the bottom trench, wherein the bottom surface of the bottom trench is in contact with the channel stop impurity-doped region.

11. (Currently Amended) The method as claimed in claim 9, wherein the pilot trench has an identical or wider width than that of the channel stop impurity-doped region.

12. (Currently Amended) A method of forming semiconductor devices having field isolation layers in trenches comprising:
providing a semiconductor substrate having a first region and a second region;
forming a pilot trench in the second region;
forming in a single step, a first trench in the first region and enlarging the pilot trench to form a second trench composed of an upper trench and a bottom trench at the bottom of the upper trench; and
forming a first field isolation layer filling the first trench and a second field isolation layer filling the second trench,
wherein the first trench and the upper trench have identical depths from a surface of the semiconductor substrate and the upper trench has a wider width than that of the bottom trench.

13. (Previously presented) The method as claimed in claim 12, wherein forming the first trench and the second trench comprises:
forming a trench mask layer on the semiconductor substrate having the pilot trench;
 patterning the trench mask layer to form a first opening exposing a predetermined region of the semiconductor substrate at the first region and a second opening exposing the

pilot trench and a predetermined region of the semiconductor substrate at both sides of the pilot trench at the second region; and

anisotropically etching the semiconductor substrate and a bottom surface of the pilot trench exposed by the first opening and the second opening to form the first trench and the second trench,

wherein the upper trench has substantially the same width as the second opening and the bottom trench has substantially the same width as the pilot trench.

14. (Previously presented) The method as claimed in claim 12, wherein after forming the pilot trench, the method further comprising forming a channel stop impurity-doped region in the semiconductor substrate apart from a bottom surface of the pilot trench with a predetermined depth, wherein a bottom surface of the bottom trench is in contact with the channel stop impurity-doped region.

15. (Previously presented) The method as claimed in claim 14, wherein the pilot trench has substantially the same width as the channel stop impurity-doped region.

16. (Previously presented) The method as claimed in claim 15, wherein forming of the pilot trench and the channel stop impurity-doped region comprises:

- forming a pilot trench mask layer on the semiconductor substrate;
- forming a pilot trench opening exposing a predetermined region of the semiconductor substrate at the second region by patterning the pilot trench mask layer;
- forming the pilot trench by etching the exposed semiconductor substrate;
- forming a channel stop impurity-doped region in the semiconductor substrate apart from a bottom surface of the pilot trench with a predetermined region by implanting impurity ions using the patterned pilot mask layer as a mask; and
- removing the patterned pilot trench mask layer.

17. (Currently Amended) The method as claimed in claim 14, wherein the pilot trench has a wider width than that of the channel stop impurity-doped region.

18. (Currently Amended) The method as claimed in claim 17, wherein forming the channel stop impurity-doped region comprises:

forming an ion-implantation mask layer on the semiconductor substrate having the pilot trench;

forming an ion-implantation opening having a narrower width than that of the pilot trench and exposing a predetermined region of a bottom surface of the pilot trench by patterning the ion-implantation mask layer;

forming a channel stop impurity-doped region in the semiconductor substrate apart from a bottom surface of the pilot trench with a predetermined depth by implanting impurity ions using the patterned ion-implantation mask layer as a mask; and

removing the patterned ion-implantation mask layer.

19. (Currently amended) The method as claimed in claim 12, wherein forming the first trench and the second trench comprises:

forming ~~a~~the first trench at a predetermined region of the semiconductor substrate at the first region and ~~an~~the upper trench at a predetermined region of the semiconductor substrate at the second region; and

forming ~~a~~the bottom trench by selectively etching a predetermined region of a bottom surface of the upper trench.

20. (Original) The method as claimed in claim 19, further comprising forming a channel stop impurity-doped region under a bottom surface of the bottom trench, wherein the bottom surface of the bottom trench is in contact with the channel stop impurity-doped region.

21. (Original) The method as claimed in claim 20, wherein a width of the bottom trench is equal to or wider than that of the channel stop impurity-doped region.

22. (Currently Amended) A method of forming semiconductor devices having field oxides layers in trenches comprising:

providing a semiconductor substrate having a first region, a second region and a key region;

forming a pilot trench at a predetermined region of a semiconductor substrate at the second region and an initial key trench at a predetermined region of the semiconductor substrate at the key region;

forming a trench mask layer on a surface of the semiconductor substrate having the pilot trench and the key trench;

patterned the trench mask layer to form a first opening exposing a predetermined region of the semiconductor substrate at the first region, a second opening exposing the pilot trench and a predetermined region of the semiconductor substrate at both sides of the pilot trench the second region and a key opening exposing the initial key trench and a predetermined region of the semiconductor substrate at the key region;

anisotropically etching the bottom surface of the pilot trench and the exposed semiconductor substrate to form a first trench at the first region, a second trench composed of an upper trench at a surface of the semiconductor substrate at the second region and a bottom trench at a bottom surface of the upper trench, and a key trench composed of an upper key trench at a surface of the semiconductor substrate at the key region and a bottom key trench at a bottom surface of the upper key trench; and

forming a first field oxide layer in the first trench, a second field oxide layer in the second trench and a key field oxide layer in the key trench,

wherein the first trench, the upper trench and the upper key trench have identical depths from a surface of the semiconductor substrate, the upper trench has substantially the same width as the second opening and the bottom trench has substantially the same width as the pilot trench.